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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/78, 29/60

A1

(11) International Publication Number: WO 97/07548

(43) International Publication Date: 27 February 1997 (27.02.97)

(21) International Application Number: PCT/US96/13039

(22) International Filing Date: 15 August 1996 (15.08.96)

(30) Priority Data:
537,156 21 August 1995 (21.08.95) US

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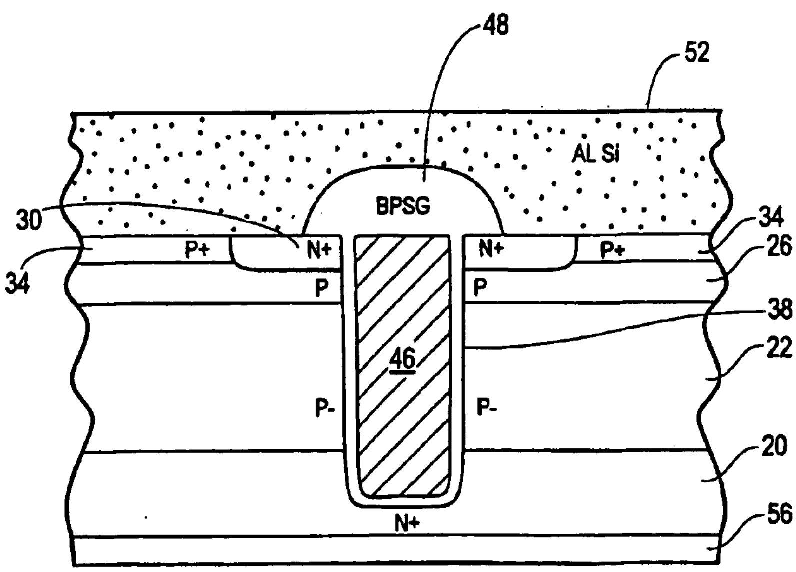
(81) Designated States: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
With amended claims.

(54) Title: LOW VOLTAGE SHORT CHANNEL TRENCH DMOS TRANSISTOR



(57) Abstract

A low voltage trench DMOS transistor has simplified punch-through elimination, improved safe operating area and threshold control. The DMOS transistor includes (for an N-channel device), from the top side down, an N+ source region (30), a P-body region (26), a P-drift region (22) and an N+ drain region (20). The trench (38) penetrates down into the drain region (20), with the gate electrode located in the trench (38). When the transistor is reverse-biased, the depletion region spreads from the drain region into the P-drift region (22). The thickness of the drift region determines the drain-source breakdown voltage. Diffusing the body region into the drift region (22) allows control of both the surface concentration in the channel region and the channel length, resulting in improved threshold control. Thus this device has a short channel and a low threshold voltage. A complement P-channel device has similar advantages.

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LOW VOLTAGE SHORT CHANNEL TRENCH DMOS TRANSISTOR

FIELD OF THE INVENTION

This invention pertains to semiconductor devices and more specifically to a trenched DMOS transistor suitable for use as a power transistor and having punch-through elimination, improved safe operating area and threshold control.

DESCRIPTION OF THE PRIOR ART

DMOS transistors are well known and are especially suitable for use as power transistors. Such transistors are typically fabricated by well known semiconductor fabrication techniques. A typical power transistor includes hundreds or thousands of cells formed in a single semiconductor substrate and connected together electrically. Prior art DMOS transistors have several well known deficiencies, including having punch-through i.e. current conduction from the source region to drain region, when such is not desired. Also there is the deficiency of control of the threshold voltage. Additionally, such devices often suffer from excessive resistance of the pinched body region, which tends to cause latchback (i.e. snap back).

SUMMARY

In accordance with the invention, a vertical DMOS field effect transistor includes (for an N-channel device) a N+ drain region overlain by a P- drift region which in turn is overlain by a P body region which is overlain by a N+ source region. A trench penetrates through the source region, body region and drift region into the drain region and is filled with a conductive polycrystalline silicon gate electrode. The trench penetrating down into the drain region is useful in

accordance with the present invention due to the need to invert the entire trench sidewall surface. A source-body contact overlies the principal surface of the silicon and is in electrical contact with the source region and is also in electrical contact with the body region via a P+ body contact formed in an upper portion of the P body region.

Advantageously this structure provides a power transistor device with a simplified punch-through elimination structure, improved safe operating area, and threshold control. The device has a short channel and a low threshold voltage for e.g. low voltage battery applications.

When the device is reverse-biased, the depletion region spreads from the N+ drain region into the P- drift region. The thickness of this P- drift region in conjunction with the thickness and concentration of the P body region determines the drain-source breakdown voltage. Diffusing the P body region into the P- drift region allows control of both the surface concentration in the channel region and the channel length, resulting in improved threshold control. For safe operating area, the effective body junction depth is the combination of the body and drift regions, resulting in lower Rb′.

When the device is forward biased, the gate voltage easily inverts the surface of the drift region. Since critical electric field has been achieved in the body (channel) region, carriers are injected into the drift region with maximum velocity which results in low resistance for this region.

A complementary P-channel device which is otherwise similar structurally has also been found to be advantageous. In another N-channel embodiment a P+ doped "body plus" region is provided which extends from the principal surface of the semiconductor material

adjacent the source region into the drift region.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross-section of a semiconductor device in accordance with the present invention.

Fig. 2 shows a cross-section of a second embodiment of a semiconductor device in accordance with the present invention.

Figs. 3A-3C show process steps for forming a semiconductor device in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 shows a trenched DMOS transistor in accordance with the present invention. It is to be understood that this shows one cell of what is typically many cells (as described above) of a transistor. Also conventionally this cross sectional depiction shows various semiconductor regions delineated by lines. It is to be understood that in an actual device there are concentration gradients between these regions. Moreover, Fig. 1, as is true of the other figures in this disclosure, is not to scale and shows only an active portion of the transistor. The surrounding termination region is discussed below. Moreover, the description of various materials, dimensions, doping levels, etc. herein is intended to be illustrative and not limiting; other materials, dimension, and doping levels may also be used in accordance with the present invention as is well known in the field.

The transistor of Fig. 1 in its lower portion includes an N+ doped drain region 20 having typically a dopant concentration of $2 \times 10^{19}/cm^3$. It is to be understood that Fig. 1 depicts an N-channel device and the complementary P-channel device may also be

fabricated with all the conductivity types being opposite to that shown in Fig. 1. Such a complementary P-channel device would have comparable performance to that of the depicted N-channel device.

Overlying the N+ drain region 20 is a P- drift region 22, the thickness of which partially determines the drain/source breakdown voltage of the device. For instance, for a 30 volt device the P- drift region 22 has e.g. a thickness of 2 μm; for a ten volt device a thickness of 1 μm is sufficient. P- drift region 22 is typically an epitaxial layer grown on an N+ doped substrate 20. The drift region 22 is lightly doped, typically having a resistivity of 20 ohm cm and a doping concentration of $7 \times 10^{14}/cm^3$.

In the upper portion of the epitaxial layer is a diffused P body (channel) region 26 typically 0.6 to 1.1 μm thick and having a typical compensated surface doping concentration in the range of 1 to 3 x $10^{16}/cm^3$. The thickness and doping level of this body region 26 is important because its properties determine the length of the channel. Also diffused into the upper portion of the epitaxial layer is the N+ source region 30 having a typical thickness of 0.2 to 0.5 micrometer and a surface doping concentration of $5 \times 10^{19}/cm^3$. Formed also in the upper portion of the epitaxial layer and adjacent the source region 30 is a P+ body contact region 34 allowing ohmic contact to be made to the body region 26. The P+ body contact region 34 has a thickness similar to that of the source region 30 and a typical surface doping concentration of $5 \times 10^{18}/cm^3$.

A trench 38, typically 2 to 3 μm deep and 1 μm wide, penetrates into the drain region 20. Trench 38 is conventionally lined with a gate oxide layer 42 and filled with a doped polysilicon gate electrode 46. A layer 48 of boro-phosphosilicate glass (BPSG) overlies and insulates the upper portion of the conductive gate

electrode 46. A conventional aluminum silicon metallization layer 52 overlies the BPSG layer and electrically contacts both the source region 30 and the body contact region 34. Also conventionally present is a passivation layer (not shown) overlying the metallization layer and a drain metallization layer 56 formed on the lower portion of the substrate to electrically contact the drain region 20.

The structure shown in Fig. 1 therefore includes, arranged vertically, semiconductor regions including a source region 30, a body region 26, a drift region 22 and a drain region 20. There is known in the art a lateral DMOS with similar semiconductor regions but of course arranged laterally rather than vertically. Advantageously, the vertical device of Figure 1 saves considerable chip "real estate" (surface area) over a comparable lateral device.

Advantageously the present device allows spreading of the breakdown between the drain and the drift region and not across the channel. Thus, a shorter channel is formed than in other types of semiconductor devices. In the case of the device of Fig. 1, the channel is in the body region 26 between the source region 30 and the drift region 22. This device therefore allows use of a short channel without the problem of punch-through.

As is known, in prior art trenched DMOS devices when one grows gate oxide over an N- doped drift region, surface accumulation occurs, i.e. the N- region becomes more N-type and this undesirably compensates the P-body region and shortens the channel even more, leading to punch through. The present device avoids this by providing an enhancement in the opposite direction because the P- drift region 22 depletes at the conduction surface next to the gate oxide, so that the channel experiences less effect from the redistribution of charge at the conduction surface.

The present device also avoids the problem of latchback (snap back) which is typically caused by the resistance Rb′ of the body region 26. When the device is reverse biased, the leakage current through Rb′ causes a voltage gradient along the source/P body junction. When this junction becomes forward biased, the NPN parasitic transistor latches. The parasitic transistor is the NPN (bipolar) transistor formed by source 30, body and drift regions 26 and 22, and drain region 20. Since the present device has a vertically wider effective body (regions 22, 26), Rb′ advantageously is decreased.

When the device of Fig. 1 is reverse biased, the depletion region spreads from the drain region 20 into the drift region 22. The thickness of the drift region 22 determines the drain to source breakdown voltage. Formation by diffusion of the body region 26 into the drift region 22 improves control of both the surface concentration and the body region concentration and the resulting channel length, and improves the threshold control. For safe operating area, the effective body junction depth is that of the combined drift 22 and body regions 26, resulting in lower Rb′.

When the device of Fig. 1 is forward biased, the gate voltage easily inverts the conduction surface next to the gate oxide of the drift region 22. Since critical electric field has been achieved in the channel (body) region 26, carriers are injected into the drift region 22 with maximum velocity, resulting in lower resistance for the drift region.

A top side geometry (not shown) suitable for the device of Fig. 1 is any of the well known types of cells, i.e. circular, rectangular, hexagonal, linear, etc.

A second embodiment in accordance with the present invention is shown in Fig. 2, the structure of which is

generally identical to those of Fig. 1 (although two trenches are shown rather than one for greater understanding). Thus trench 38B, gate electrode 46, and BPSG layer 48A in Fig. 2 correspond to structures 38, 46, 48 in Fig. 1 and trench 38B, gate electrode 46B, and BPSG layer 48B are the second trench and associated structures. Fig. 2 shows the additional P+ "body plus" region 62A, 62B formed between two portions of the source region 30 and extending at portion 62A not only into the upper portion of the body region 26 to serve as a body contact, but also extending down at portion 62B into the drift region 22. The doping level of body plus region 62A, 62B is the same or even heavier than that of the body contact region 34 in Fig. 1.

Fabrication of the embodiment of Fig. 2 is compatible with processes already used in the semiconductor industry and provides better control (prevents latchback) of the NPN parasitic transistor present. However, the embodiment of Fig. 2 has a potential detriment in that the breakdown voltage may be compromised by the distance from the body plus region 62B to the drain region 20 i.e., these two regions approach relatively close together, hence providing a potential breakdown path.

Also shown in Fig. 2 is an example of a termination structure which in this case is a polysilicon field plate 66 in the righthand portion of the drawing. The field plate 66 is located on the principal surface of the semiconductor substrate and is in contact with the P+ region 34 to the right of trench 38A. P+ region 34 is a channel stop to prevent conduction. A metallization layer 52B overlies field plate 60, but is isolated from metallization layer 52. This termination structure is also suitable for use with the transistor of Fig. 1.

Another termination structure (not shown) suitable for use with the transistors of Fig. 1 and Fig. 2 is a trench which penetrates (like the trenches in the active region) through the epitaxial layer down into the drain region but having a dummy cell (one not having any N+ source region) in the (exterior) termination portion of the transistor. This second termination structure would typically include a conductive polysilicon gate runner (not shown) which connects to the polysilicon in the termination trench and to the active gate electrodes. One advantage therefore in accordance with the present invention is the ability to use such relatively simple termination structures.

A process flow to fabricate a transistor as in Fig. 1 (or Fig. 2) is described hereinafter with reference to Fig. 3A and following. It is to be understood that this process flow is illustrative and not limiting and other process flows may also be used to fabricate a transistor in accordance with the present invention.

1. A conventional silicon substrate 20 is provided in Fig. 3A which is N+ doped to a concentration of $2x10^{19}/cm^3$.

2. An epitaxial layer 22 approximately 4 μm thick is grown on the upper portion of the substrate. This epitaxial layer is lightly P- doped and has a resistivity of 20 ohm.cm.

3. An oxide layer (not shown) is grown 6,000 Å thick over the principal surface of the epitaxial layer. The first mask layer (not shown) is formed over the surface of this oxide layer. The mask is patterned and the oxide layer then etched. This mask thereby defines the active portions of the transistor.

4. In the second mask step, another mask layer 70 is formed on the principal surface and patterned to

define the locations of the gate trenches.

5. The gate trench is 38 anisotropically etched to a depth of 2 to 3 μm and a width of 1 μm in Fig. 3B and mask layer 70 is stripped.

6. Gate oxide layer 42 is grown to a thickness of 100 to 700Å over the sidewalls and floors of the trench and also over the principal surface of the substrate.

7. Polycrystalline silicon 72 (polysilicon) is deposited in the trench 38 and over the silicon principal surface to a thickness of 15,000Å and on the drain 20 surface of the silicon.

8. The polysilicon is then removed from the backside (drain) surface of the substrate, and any oxide on the backside surface is also removed.

9. In Fig. 3C, the polysilicon is then etched back (planarized) to a final thickness of 5,500Å.

10. The polysilicon is N-doped using for instance phosphorous.

11. Next is the polysilicon masking step in which a photoresist mask layer (not shown) is formed thereover and patterned to define the gate electrodes and gate runners. In this step the polysilicon, after the mask is patterned, is etched down so that the polysilicon gate electrode 46 does do not protrude above the level of the substrate at the trench 38 (the polysilicon 46 is planarized with the silicon principal surface). The photoresist is then stripped.

12. Next is a blanket implant of the P body region 26 using a dose of 5×10^{13} to $10^{14}/cm^2$ of boron at 50 KeV energy.

13. The P body region 26 is diffused (driven in) so as to form a 500Å thick oxide layer (not shown) during the drive-in process. The doping concentration of the P body region 26 is intended to be in one embodiment 1 to $3 \times 10^{16}/cm^3$ doping level at its surface

next to the gate oxide.

An unmasked (blanket) etch is performed to etch back this 500 Å oxide layer to a thickness of 250 to 300 Å.

14. Next is the formation and patterning of the N+ source region mask (not shown).

15. The source region 30 is implanted using this source region mask using a dose of 8 x $10^{15}/cm^2$ at 80 KeV of arsenic.

16. The source region 30 is diffused (driven in) so as to grow a 1,600Å thick oxide layer.

17. The BPSG layer is deposited; the BPSG is doped lightly with phosphorous and boron. (This step and the remaining steps are not depicted, being conventional).

18. The BPSG layer is flowed.

19. Next is the formation and patterning of the contact mask. This determines the locations of the P+ body contact regions.

20. Using the contact openings, the P+ body contact regions are implanted. For the embodiment of Fig. 2 where it is desired to have the body plus region, this implantation is at a dose of $3x10^{15}/cm^2$ at 50 KeV of boron so as to achieve a final surface concentration of $10^{19}/cm^3$. This forms the ohmic body contact. (For the Fig. 1 embodiment this implantation is at a dose of $10^{15}/cm^2$ at 50 KeV.)

21. The BPSG is reflowed (smoothed out). This reflow step also activates the P+ body contact region implant.

22. An unmasked oxide etch is performed to clear out the contact holes in the BPSG layer, to remove the oxide and any material present due to the reflow process.

23. An aluminum silicon metal layer is deposited to a thickness of e.g. 2.8 μm over the entire

structure.

24. A metal mask layer is formed and patterned and the metal layer is etched accordingly to define the metallization.

25. A passivation layer of PSG is formed over the entire structure.

26. A pad mask layer is formed and patterned and the PSG passivation layer patterned thereby to expose the contact pads.

27. The aluminum/silicon is alloyed.

28. Next there is a back lap of the backside of the substrate.

29. Last is the backside metallization deposit to form the drain electrode.

While particular structures and processes are disclosed herein, these are not intended to be limiting. Furthermore, a transistor in accordance with the present invention may be used for applications other than the above-described low voltage application; as is well known, the voltage which the device will withstand is typically limited by the trench and semiconductor region configurations. Particular advantages in accordance with the present invention are that one can achieve a lower threshold voltage and short channel without punch through; improved threshold control due to the P drift region; and the ability to use a relatively simple termination structure, rather than the more complex termination structures often used with field effect transistors for power applications.

This disclosure is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of this disclosure and are intended to fall within the scope of the appended claims.

We claim

1. A semiconductor device formed in a semiconductor material, comprising:

a drain region of a first conductivity type;

a drift region of a second conductivity type overlying the drain region;

a body region of the second conductivity type and doped to a higher concentration than the drift region, and overlying the drift region;

a source region of the first conductivity type overlying the body region and extending to a principal surface of the semiconductor material; and

a conductive gate electrode formed in a trench extending into the semiconductor material from the principal surface through the source region, body region, and drift region and the trench extending into the drain region.

2. The semiconductor device of Claim 1, wherein the channel region has a thickness in a range of 0.3 to 0.8 μm.

3. The semiconductor device of Claim 1, wherein the body region has a thickness in a range of 1.0 to 3 μm.

4. The semiconductor device of Claim 1, wherein the source region has a thickness in a range of 0.1 to 0.7 μm.

5. The semiconductor device of Claim 1, further comprising a body contact region of the second conductivity type and of higher doping concentration than the channel region, extending from the principal surface to the body region and being adjacent the

source region.

6. The semiconductor device of Claim 5, wherein the body contact region extends into the drift region.

7. The semiconductor device of Claim 1, wherein the drift region is an epitaxial layer formed on the drain region.

8. The semiconductor device of Claim 1, wherein a peak doping level of the body region is in a range of $10^{16}/cm^3$ to $3 \times 10^{16}/cm^3$.

9. The semiconductor device of Claim 1, further comprising a termination structure laterally surrounding an active portion of the semiconductor device and including:

a trench formed in the semiconductor material and extending into the drain region; and

a conductive structure formed in the trench and being connected to the gate electrode.

10. A method of operating a trenched transistor, having arranged vertically, alongside a gate electrode in the trench, a source region, a body region, a drift region and a drain region, comprising the steps of:

reverse-biasing the transistor;

when the transistor is reverse-biased, spreading a depletion region from the drain region into the drift region, thereby increasing the drain region to source region breakdown voltage;

forward-biasing the transistor; and

when the transistor is forward biased, inverting a surface of the drift region adjacent the trench, thereby reducing a resistance of the drift region.

11. A method of fabricating a trenched semiconductor device, comprising the steps of:

providing a semiconductor substrate having a first conductivity type;

forming a drift region on an upper portion of the substrate, the drift region having a second opposite conductivity type;

forming a body region overlying the drift region, the body region having the second conductivity type and being more heavily doped than the drift region;

forming a source region in an upper portion of the body region, the source region having the first conductivity type;

forming a trench penetrating through the source region, the body region, the drift region and into the substrate;

forming a conductive gate electrode in the trench; and

forming an electrical contact overlying and in contact with the source region.

12. The method of Claim 11, wherein the drift region has a thickness in a range of 1 to 2 μm.

13. The method of Claim 11, wherein the body region has a thickness in a range of 0.5 to 3 μm.

14. The method of Claim 11, wherein the source region has a thickness in a range of 0.1 to 0.7 μm.

15. The method of Claim 11, further comprising forming a body contact region of the second conductivity type and of higher doping concentration than the body region, the body contact region extending from the principal surface to the body region and being

adjacent the source region.

16. The method of Claim 15, wherein the body contact region extends into the drift region.

17. The method of Claim 11, wherein the step of forming the drift region comprises growing an epitaxial layer on the drain region.

18. The method of Claim 11, wherein a doping level of the body region is in a range of $10^{16}/cm^3$ to 3 x $10^{16}/cm^3$.

19. The method of Claim 11, further comprising forming a termination structure laterally surrounding an active portion of the semiconductor device and further including the steps of:

forming a trench in the semiconductor material and extending into the drain region; and

forming a conductive structure in the trench and connected to the gate electrode.

AMENDED CLAIMS

[received by the International Bureau on 29 October 1996 (29.10.96); original claim 3 cancelled; original claims 1,2,5,8 and 10 amended; new claims 20 and 21 added; remaining claims unchanged (4 pages)]

1. A low voltage semiconductor device formed in a semiconductor material, comprising:

a drain region of a first conductivity type;

a drift region of a second conductivity type overlying the drain region;

a body region of the second conductivity type and doped to a higher concentration than the drift region, and overlying the drift region;

a source region of the first conductivity type overlying the body region and extending to a principal surface of the semiconductor material; and

a conductive gate electrode formed in a trench extending into the semiconductor material from the principal surface through the source region, body region, and drift region and the trench extending into the drain region, wherein the device has a breakdown voltage of 30 volts or less.

2. The semiconductor device of Claim 1, wherein the body region has a thickness in a range of 0.6 to 1.1 μm.

3. (Canceled)

4. The semiconductor device of Claim 1, wherein the source region has a thickness in a range of 0.1 to 0.7 μm.

5. The semiconductor device of Claim 1, further comprising a body contact region of the second conductivity type and of higher doping concentration than the body region, extending from the principal surface to the body region and being adjacent the source region.

6. The semiconductor device of Claim 5, wherein the body contact region extends into the drift region.

7. The semiconductor device of Claim 1, wherein the drift region is an epitaxial layer formed on the drain region.

8. The semiconductor device of Claim 1, wherein a peak doping level of the body region is in a range of $1 \times 10^{16}/cm^3$ to $3 \times 10^{16}/cm^3$.

9. The semiconductor device of Claim 1, further comprising a termination structure laterally surrounding an active portion of the semiconductor device and including:

a trench formed in the semiconductor material and extending into the drain region; and

a conductive structure formed in the trench and being connected to the gate electrode.

10. A method of operating a trenched transistor at a low voltage, having arranged vertically, alongside a gate electrode in the trench, a source region, a body region, a drift region and a drain region, comprising the steps of:

applying a voltage to the source and drain regions so as to reverse-bias the transistor;

when the transistor is reverse-biased, spreading a depletion region from the drain region into the drift region, increasing the drain region to source region breakdown voltage to no more than 30 volts;

applying a voltage to the source and drain regions so as to forward-bias the transistor; and

when the transistor is forward biased, inverting a surface of the drift region adjacent

AMENDED SHEET (ARTICLE 19)

the trench, thereby reducing a resistance of the drift region.

11. A method of fabricating a trenched semiconductor device, comprising the steps of:

providing a semiconductor substrate having a first conductivity type;

forming a drift region on an upper portion of the substrate, the drift region having a second opposite conductivity type;

forming a body region overlying the drift region, the body region having the second conductivity type and being more heavily doped than the drift region;

forming a source region in an upper portion of the body region, the source region having the first conductivity type;

forming a trench penetrating through the source region, the body region, the drift region and into the substrate;

forming a conductive gate electrode in the trench; and

forming an electrical contact overlying and in contact with the source region.

12. The method of Claim 11, wherein the drift region has a thickness in a range of 1 to 2 μm.

13. The method of Claim 11, wherein the body region has a thickness in a range of 0.5 to 3 μm.

14. The method of Claim 11, wherein the source region has a thickness in a range of 0.1 to 0.7 μm.

15. The method of Claim 11, further comprising forming a body contact region of the second

conductivity type and of higher doping concentration than the body region, the body contact region extending from the principal surface to the body region and being adjacent the source region.

16. The method of Claim 15, wherein the body contact region extends into the drift region.

17. The method of Claim 11, wherein the step of forming the drift region comprises growing an epitaxial layer on the drain region.

18. The method of Claim 11, wherein a doping level of the body region is in a range of $10^{16}/cm^3$ to $3 \times 10^{16}/cm^3$.

19. The method of Claim 11, further comprising forming a termination structure laterally surrounding an active portion of the semiconductor device and further including the steps of:

forming a trench in the semiconductor material and extending into the drain region; and

forming a conductive structure in the trench and connected to the gate electrode.

20. The semiconductor device of Claim 1, wherein the drift region has a thickness in a range of 1 to 2 μm.

21. The semiconductor device of Claim 1, further comprising a plurality of identical such devices formed in a single substrate, the drift region of each device extending to a drift region of an adjacent device.

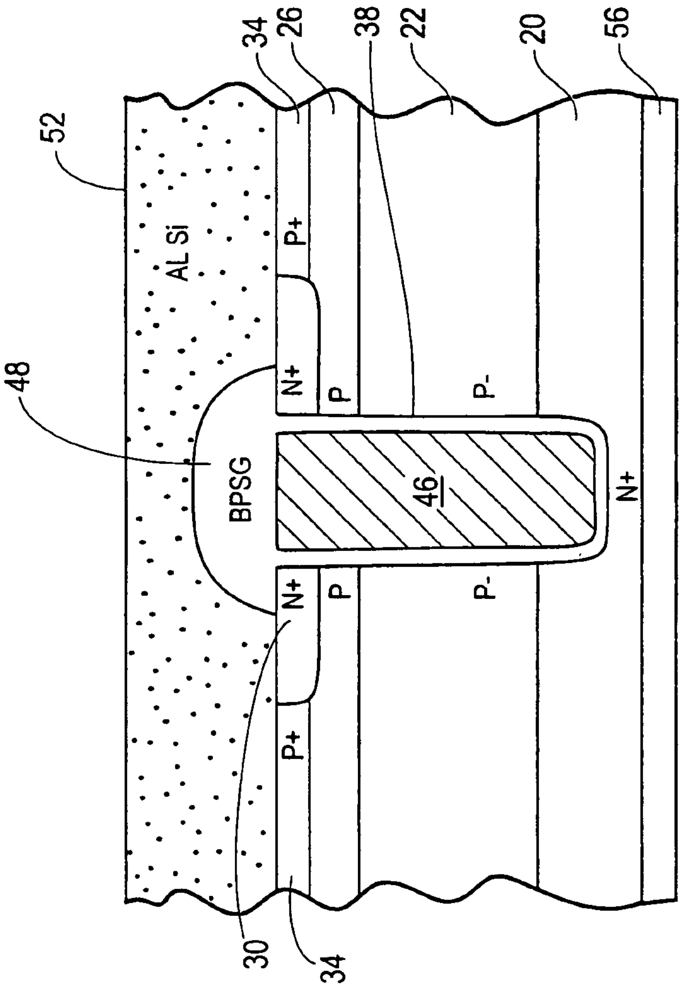
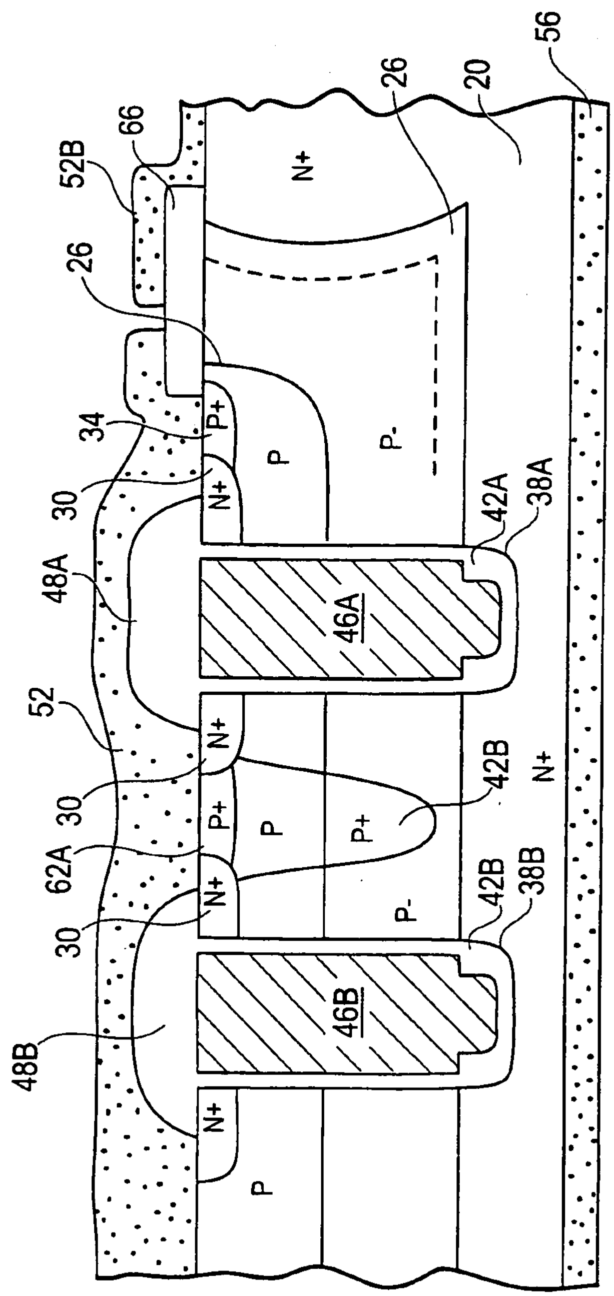


FIG. 1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P

FIG. 2

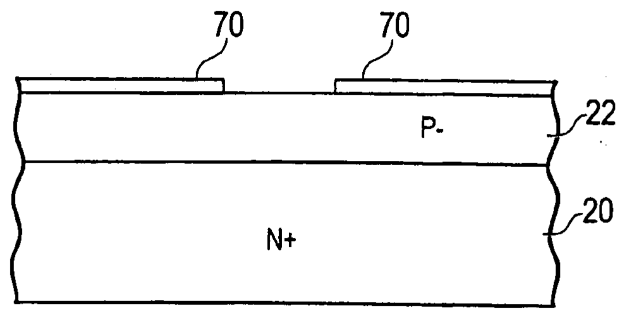

FIG. 3A

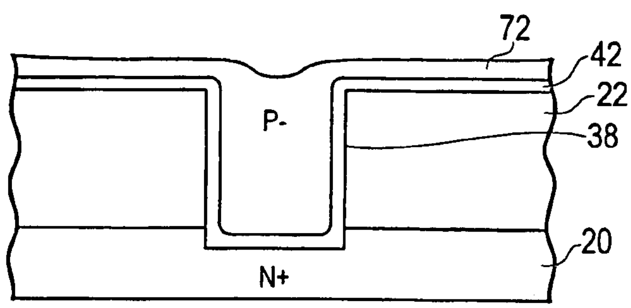

FIG. 3B

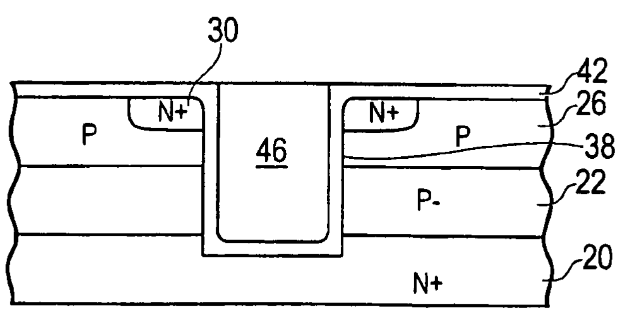

FIG. 3C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/13039

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 29/78;H01L 29/60
US CL :257/330,332,327;437/66,68
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/330,332,327;437/66,68

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	UK 2,026,239 A (MARINUS) 30 JAN 1980 (30/01/80), Page1, lines 53-57; especially Fig.2, page 2, lines 62-65; page 3, lines 25-31,54.	1,3,5-9,11 13,15-19 ---------------- 2,4,10,12, 14
Y	EP 0,580,452 A1 (CHANG) 26 JAN 1994 (26/01/94), column 3, lines 23-27	2,4,12,14
Y	US 5,341,011 (HSHIEH et al) 23 AUG 1994 (23/08/94), Column 1, lines 7-13.	10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 SEPTEMBER 1996	26 SEP 1996

Name and mailing address of the ISA/US	Authorized officer
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